REMARKS

This application has been carefully reviewed in light of the final Office Action dated February 9, 2006. Claims 4-6, 8-11, 13-15 and 17-19 remain pending in this application. Claims 4, 5, 13 and 14 are the independent claims. Claims 4-6 and 8-11 have been amended. Claims 1-3, 7, 12, 16 and 20-25 have been canceled without prejudice. It is believed that no new matter is involved in the amendments or arguments presented herein. Reconsideration and entrance of the amendment in the application are respectfully requested.

Interview Summary

Applicant thanks the courtesy extended by the Examiner during telephone interview conducted on May 25, 2007. Applicant has incorporated the substance of the interview in the present response.

Response to Advisory Action

Advisory Action dated May 3, 2007 indicates the amended Claims 4-6 and 8-11 in the after final response filed April 30, 2007 are not entered and considered. Accordingly, Applicant is submitting those amended claims in the present response. Entrance and reconsideration of the amended Claims 4-6 and 8-11 are respectfully requested.

Art-Based Rejections

Claims 4, 6, 10, 11, 13-15, and 19 were rejected under 35 U.S.C. § 103(a) over U.S. Patent Pub. No. 2002/0126719 A1 (Kadota) in view of WO 02/89223 (Ishizaki); claim 5 was rejected under § 103(a) over Kadota in view of Ishizaki and U.S. Patent No. 6,084,899 (Shakuda); Claims 8-9 and 17-18 were rejected under § 103(a) over

Kadota in view of Ishizaki as applied to claim 13, and further in view of U.S. Patent No. 6,787,435 B2 (Gibb).

Applicant respectfully traverses the rejections and submits that the claims herein are patentable in light of the arguments below.

The Kadota Reference

Kadota is directed to a semiconductor photonic device having GaN-based compound semiconductor layer as an active buffer layer (*Kadota; para. [0002]*).

The Ishizaki Reference

Ishizaki is directed to a method of fabricating a light emitting device having a light emitting layer portion which includes a p-type $Mg_xZn_{1-x}O$ layer. The p-type $Mg_xZn_{1-x}O$ layer is grown by a metal organic vapor-phase epitaxy process while supplying organometallic gases, an oxygen component source gas and a p-type dopant gas into a reaction vessel, and is annealed during and/or after completion of the growth thereof in an oxygen-containing atmosphere (*Ishizaki; para. [0015]*).

The Shakuda Reference

Shakuda is directed to a semiconductor light emitting device of double hetero junction including an active layer and clad layers. The clad layers include an n-type layer and p-type layer. The clad layers sandwich the active layer. A band gap energy of the clad layers is larger than that of the active layer. The band gap energy of the n-type clad layer is smaller than of the p-type clad layer (*Shakuda; Abstract*).

The Gibb Reference

Gibb is directed to a light-emitting element. According to Gibb, a light emitting diode (LED) includes a sapphire substrate (26) having front and back sides (33, 35), and a plurality of semiconductor layers (28, 30, 32) deposited on the front side (33) of the sapphire substrate (26). The semiconductor layers (28, 30, 32) define a light-emitting structure that emits light responsive to an electrical input. A metallization stack (40) includes an adhesion layer (34) deposited on the back side (35) of the sapphire substrate (26), and a solderable layer (38) connected to the adhesion layer (34) such that the solderable layer (38) is secured to the sapphire substrate (26) by the adhesion layer (34). A support structure (42) is provided on which the LED is disposed. A solder bond (44) is arranged between the LED and the support structure (42). The solder bond (44) secures the LED to the support structure (42). (*Gibb; Abstract*).

The Claims are Patentable Over the Cited References

The present application is generally directed to light emitting devices having transparent electrodes that inhibit degradation.

As defined by amended independent Claim 4, an electrode structure includes a transparent electrode including ZnO. An Mg-doped ZnO film formed on the electrode. The electrode is disposed on a semiconductor device.

The applied references do not disclose or suggest the features of present invention as recited in the claims. In particular, the applied references do not disclose or suggest "a transparent electrode including ZnO; and an Mg-doped ZnO film formed on the electrode" recited in amended independent Claim 4. Moreover, the applied references do not disclose or suggest, "[T]he electrode is disposed on a semiconductor device," recited in amended independent Claim 4.

Kadota does not disclose or suggest ZnO electrode, let alone the Mg-doped ZnO transparent electrode film formed on the electrode. In Advisory Action dated May 3, 2007, the Office argues that the buffer layer **43** is the ZnO electrode (*Kadado FIG. 4*). Kadota expressly teaches a p-type electrode **50** and n-type electrode **49** (*Kadota at [0029]; FIG. 2; also see FIG. 2, reference elements 27 and 26; FIG. 4 reference elements 50 and 49; FIG. 5, reference elements 57 and 56*). Electrode is an input/output terminal of a device, and that definition is well known by persons of ordinary skill in the art. Expanding the well-know structure to a buffer layer is unsupported by Kadota or general knowledge in the art.

In particular, the Office Action argues the buffer layer **43** is an electrode for being of a low resistivity layer and of the same electrical potential the electrode **49** (*see Advisory Action*). That construction of "electrode" is unreasonable broad. For example, an electrode often connects to a wire, and that wire provides electrical signal to and from the electrode. That wire is also of low resistivity and of the same electrical potential as the electrode. However, persons of ordinary skill in the art would not confuse the wire and the electrode. Accordingly, the Office Action's construction of "electrode" is unreasonably broad. Reconsideration of that construction is thus respectfully requested.

Even if the buffer layer **43** is an electrode, Kadota still fails to disclose or suggest that ZnO electrode being formed on a semiconductor device as recited in amended independent Claim **4**. The Office Action identifies layers **44-48** of FIG. **4** of Kadota as a semiconductor device. However, the ZnO buffer layer **43**, identified as the electrode recited in amended independent Claim **4**, is disposed between the layers **44-48** (the semiconductor device according to the Office Action) and the substrate **42**. Moreover, Kadota teaches that the layers **44-48** are etched away for forming the electrode (*Kadota Para. [0037] recites "...the Zno buffer layer **43** ... is*

partially exposed for forming the electrode."). Accordingly, Kadata does not disclose the ZnO electrode being disposed on a semiconductor device as recited in amended independent Claim 4.

In contrast, amended independent Claim 4 recites that the Mg-doped ZnO film is formed a ZnO electrode, which is disposed on the most outer surface of a semiconductor device. FIG. 2 of the Specification illustrates an embodiment of present invention. In that figure, the electrode **12** is disposed on the outer most surface of the semiconductor device **20**. The Mg-doped ZnO transparent electrode film **11** is disposed on the electrode. In the claimed invention, the Mg-doped ZnO transparent electrode film prevents degradation due to penetration of ion-containing moisture better than the ZnO electrode alone. Kadota does not disclose or suggest these features.

Regarding independent Claim 13, the applied references do not disclose or suggest "a semiconductor layer formed on a substrate" recited in that Claim.

In Office Action dated February 9, 2007, the upper electrode **50** of Kadota is identified as the substrate (*see page 5 of that Office Action*). Applicant respectfully submits that assertion is improper. Again, the term "substrate" is a well defined term in the art, and arbitrary expansion of the known definition of the term is improper. According to *Random House Unabridged Dictionary, © Random House, Inc. 2006*, "substrate" in electronic is defined as "a supporting material on which a circuit is formed or fabricated." The upper electrode **50** is not a "supporting material," and therefore, the construction of the upper electrode **50** as a substrate layer is improper.

In the interview, the Examiner argues the term "substrate" should be constructed under Latin meaning for "substratum." Applicant respectively notes "substratum" is also defined as something that is spread or laid under something

else (*see again Random House Unabridged Dictionary*). Again, the upper electrode **50** is not a laid under the device, and therefore cannot be a substrate layer.

In any event, the claims of applications to the United State Patent and Trademark Office should be constructed in accordance with plain usage of the English language, and not Latin. Kadota expressly identifies the layer **50** as the upper electrode and layer **42** as the substrate, contrary to the Office Action's position. In view of the Kadota's disclosure, the plain meaning of "substrate," and the dictionary definition of "substrate," Applicant respectfully submits the Office's assertion of the upper electrode **50** as the "substrate" recited in independent Claim 13 and electronic art in general is improper. Reconsideration and withdrawal of the rejection are respectfully requested.

Accordingly, Kadota fails to disclose or suggest the features of independent Claims 4 and 13. The applied ancillary references are not seen to remedy the deficiencies of Kadota.

Since the applied references fail to disclose, teach or suggest the above features recited in independent Claims 4 and 13, those references cannot be said to anticipate or render obvious the invention which is the subject matter of that claim.

Accordingly, independent Claims 4 and 13 as are believed to be in condition for allowance and such allowance is respectfully requested.

Applicant respectfully submits that independent Claims 5, 13, and 14 reciting similar features are allowable for the least the same reasons as those discussed in connection with amended independent Claim 4.

The remaining claims depend either directly or indirectly from the independent claims, and recite additional features of the invention which are

neither disclosed nor fairly suggested by the applied references are therefore also believed to be in condition for allowance. Such allowance is respectfully requested.

Conclusion

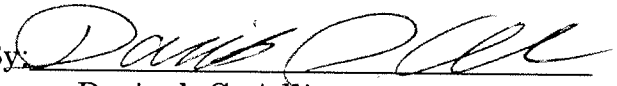
In view of the foregoing, it is respectfully submitted that the application is in condition for allowance. Reexamination and reconsideration of the application, as amended, are requested.

If for any reason the Examiner finds the application other than in condition for allowance, the Examiner is requested to call the undersigned attorney at the Los Angeles, California telephone number (310) 785-4721 to discuss the steps necessary for placing the application in condition for allowance.

If there are any fees due in connection with the filing of this response, please charge the fees to our Deposit Account No. 50-1314.

Respectfully submitted,
HOGAN & HARTSON L.L.P.

Date: June 11, 2007

By: 
Dariush G. Adli
Registration No. 51,386
Attorney for Applicant(s)

1999 Avenue of the Stars, Suite 1400
Los Angeles, California 90067
Phone: 310-785-4600
Fax: 310-785-4601